

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
2 an inductor having an impedance connected in series between an output of a
3 high frequency circuit operating at a frequency and an electrostatic discharge (ESD)
4 circuit configured to protect the high frequency circuit from an ESD event, the
5 impedance having a substantially high value at that frequency and a substantially low
6 value at the ESD event.
- 1 2. The apparatus of claim 1 wherein the ESD circuit has first and second
2 terminals, the first terminal being connected to one end of the inductor, the second
3 terminal being connected to ground.
- 1 3. The apparatus of claim 1 wherein the ESD circuit is a gate grounded
2 metal oxide semiconductor (NMOS) transistor.
- 1 4. The apparatus of claim 1 wherein the ESD circuit is a diode circuit.
- 1 5. The apparatus of claim 1 wherein the inductor is connected between a
2 first bond pad of the output and a second bond pad of the ESD circuit, the first and
3 second bond pads being on a package substrate in a package encapsulating the high
4 frequency circuit and the ESD circuit.
- 1 6. The apparatus of claim 5 wherein the inductor is connected between the
2 first and second bond pads via first and second bond wires.
- 1 7. The apparatus of claim 5 wherein the high frequency and ESD circuits
2 are on a silicon die mounted on the package substrate.
- 1 8. The apparatus of claim 5 wherein the package is one of a ball grid array
2 (BGA) package and a flip-chip package.
- 1 9. The apparatus of claim 1 wherein the frequency is higher than 1
2 gigahertz.

1 10. The apparatus of claim 1 wherein the ESD event corresponds to a low
2 frequency event.

1 11. A method comprising:
2 connecting an inductor in series between an output of the high frequency circuit
3 operating at a frequency and an electrostatic discharge (ESD) circuit configured to
4 protect the high frequency circuit from an ESD event, the inductor having an
5 impedance with a substantially high value at the frequency and a substantially low
6 value at the ESD event.

1 12. The method of claim 11 wherein connecting the inductor comprises:
2 connecting a first terminal of the ESD circuit to one end of the inductor, and
3 connecting a second terminal of the ESD circuit to ground.

1 13. The method of claim 11 wherein the ESD circuit is a gate grounded
2 metal oxide semiconductor (NMOS) transistor.

1 14. The method of claim 11 wherein the ESD circuit is a diode circuit.

1 15. The method of claim 11 wherein connecting the inductor comprises
2 connecting the inductor between a first bond pad of the output and a second bond pad
3 of the ESD circuit, the first and second bond pads being on a package substrate in a
4 package encapsulating the high frequency circuit and the ESD circuit.

1 16. The method of claim 15 wherein connecting the inductor comprises
2 connecting one end of the inductor to the first bond pad via a first bond wire; and
3 connecting an other end of the inductor to the second bond pad via a second bond wire.

1 17. The method of claim 15 wherein connecting the inductor comprises:
2 mounting a silicon die containing the high frequency and ESD circuits on the
3 package substrate.

1 18. The method of claim 15 wherein the package is one of a ball grid array
2 (BGA) package and a flip-chip package.

1 19. The method of claim 11 wherein the frequency is higher than 1
2 gigahertz.

1 20. The method of claim 11 wherein the ESD event corresponds to a low
2 frequency event.

1 21. A circuit comprising:
2 a high frequency circuit operating at a frequency, the high frequency circuit
3 having an output;
4 an electrostatic discharge (ESD) circuit configured to protect the high frequency
5 circuit from an ESD event; and
6 an inductor having an impedance connected in series between the output of the
7 high frequency circuit and the electrostatic discharge (ESD) circuit, the impedance
8 having a substantially high value at the frequency and a substantially low value at the
9 ESD event.

1 22. The circuit of claim 11 wherein the ESD circuit has first and second
2 terminals, the first terminal being connected to one end of the inductor, the second
3 terminal being connected to ground.

1 23. The circuit of claim 11 wherein the ESD circuit is a gate grounded metal
2 oxide semiconductor (NMOS) transistor.

1 24. The circuit of claim 11 wherein the ESD circuit is a diode circuit.

1 25. The circuit of claim 11 wherein the inductor is connected between a first
2 bond pad of the output and a second bond pad of the ESD circuit, the first and second
3 bond pads being on a package substrate in a package encapsulating the high frequency
4 circuit and the ESD circuit.

1 26. The circuit of claim 15 wherein the inductor is connected between the
2 first and second bond pads via first and second bond wires.

1 27. The circuit of claim 15 wherein the high frequency and ESD circuits are
2 on a silicon die mounted on the package substrate.

1 28. The circuit of claim 15 wherein the package is one of a ball grid array
2 (BGA) package and a flip-chip package.

1 29. The circuit of claim 11 wherein the frequency is higher than 1 gigahertz.

1 30. The circuit of claim 11 wherein the ESD event corresponds to a low
2 frequency event.

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